```
File   9:Business & Industry(R) Jul/1994-2006/Oct 31
         (c) 2006  The Gale Group
File  13:BAMP 2006/Oct W4
         (c) 2006  The Gale Group
File  16:Gale Group PROMT(R) 1990-2006/Nov 01
         (c) 2006 The Gale Group
File  47:Gale Group Magazine DB(TM) 1959-2006/Oct 31
         (c) 2006 The Gale group
File  88:Gale Group Business A.R.T.S. 1976-2006/Oct 31
         (c) 2006 The Gale Group
File 148:Gale Group Trade & Industry DB 1976-2006/Nov 01
         (c)2006 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 275:Gale Group Computer DB(TM) 1983-2006/Nov 01
         (c) 2006 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2006/Oct 31
         (c) 2006 The Gale Group
File 624:McGraw-Hill Publications 1985-2006/Nov 01
         (c) 2006 McGraw-Hill Co. Inc
File 634:San Jose Mercury  Jun 1985-2006/Oct 31
         (c) 2006 San Jose Mercury News
File 649:Gale Group Newswire ASAP(TM) 2006/Oct 18
         (c) 2006 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2006/Nov 01
         (c) 2006 The Gale Group

Set     Items   Description
S1     354425   CACHE? ? OR SUBCACH? OR MICROCACH? OR BUFFER? ? OR SUBBUFF-
             ER? OR MICROBUFFER?
S2    1823286   DISK? ? OR DISKETTE? OR DISC? ? OR DISCETTE? OR DISKDRIVE?
             OR DISCDRIVE? OR DISKARRAY? OR DISCARRAY? OR TAPEDRIVE? OR TA-
             PE? ?
S3    2609182   MEMORY? OR STORAGE?
S4   10089723   CONTROL???? OR MICROCONTROL? OR INTERFACE? ? OR PORT? ? OR
             ASIC? ? OR PROCESS?R? ? OR MICROPROCESS?
S5    1794821   ICC OR ICCS OR IC OR ICS OR (INTEGRATED OR MICRO)(1W)CIRCU-
             IT? ? OR CKT? ? OR MICROCIRCUIT? OR MICROCHIP? ? OR CHIP? ? OR
              SILICONCHIP?
S6    1459656   COMPUTERCHIP? OR SOC OR SEMICOND? ? OR SEMICONDUCT?R? ? OR
             SEMI()(COND? ? OR CONDUCT?R? ?)
S7     223028   (PLURALITY OR MULTIPLE OR MANY OR MULTI OR SEVERAL OR ADDI-
             TIONAL OR DIFFERENT OR SECOND OR 2ND OR NUMBER OR ALTERNATIVE-
             )(1W)S4:S6
S8     269077   (PAIR OR EXTRA OR ANOTHER OR SECONDARY OR DUAL OR THREE OR
             TWO OR PARALLEL OR REDUNDANT OR ALTERNATE OR COUPLE)(1W)S4:S6
S9      16634   (THIRD OR 3RD)(1W)S4:S6
S10   4375183   PATH? ? OR DATAPATH? OR PATHWAY? OR ROUTE OR ROUTES OR CHA-
             NNEL? ?
S11     10319   S7:S9(7N)S10
S12       592   S11(S)S1
S13       391   S12(S)(S2:S3 OR ARRAY? ?)
S14       294   S13/1992:2006
S15        97   S13 NOT S14
S16        66   RD  (unique items)
?
PLEASE ENTER A COMMAND OR BE LOGGED OFF IN 5 MINUTES
? t16/3,k/5,13,15-16,20,27

 16/3,K/5     (Item 5 from file: 16)
DIALOG(R)File  16:Gale Group PROMT(R)
(c) 2006 The Gale Group. All rts. reserv.

01532444    Supplier Number: 41869374  (USE FORMAT 7 FOR FULLTEXT)
BANYAN CERTIFIES TWO EISA SERVERS FOR VINES 02/15/91
```

Newsbytes, pN/A
Feb 15, 1991
Language: English Record Type: Fulltext
Document Type: Newswire; General Trade
Word Count: 262

... the Extended Industry Standard Architecture (EISA) bus, the units incorporate a scalable read/write-back **cache** **memory** architecture and **dual - processor** upgrade **path** to accommodate two 33-MHz 486 microprocessors and up to a megabyte of ALR ProCache **memory** on one 12-slot system board.
Tricord's PowerFrame servers were designed for local area...

16/3,K/13 (Item 4 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)
(c) 2006 The Gale group. All rts. reserv.

02433292 SUPPLIER NUMBER: 00520600
The PC Sounds Off.
Woram, J.M.
PC Magazine, v2, n3, p371-375
Aug., 1983
DOCUMENT TYPE: evaluation ISSN: 0888-8507 LANGUAGE: ENGLISH
RECORD TYPE: ABSTRACT

...ABSTRACT: sound mixing system called Diskmix, that will simultaneously maintain up to sixty-four separate recording **channels** . The system consists of a **dual** **processor** computer with two eight inch floppy drives, an intelligent **disk** controller and an IBM PC to serve as an interface between the sound engineer and...

...mixed and re-mixed in any combination using the SMPTE sync code to keep the **memory** **buffer** in sync with the audio **tape** .

16/3,K/15 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2006 The Gale Group. All rts. reserv.

05583244 SUPPLIER NUMBER: 11688330 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Drive ICs: ASICs or off-the-shelf? Cost, time-to-market pressures rule choice, say drive makers. (integrated circuits, application-specific integrated circuits)
Arnold, Bill
EDN, v36, n24A, p1(3)
Nov 28, 1991
ISSN: 0012-7515 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1641 LINE COUNT: 00130

... the buffer memory, and a controller to translate bidirectional data and perform error correction. A **second** National **Semiconductor** HPC controls the servo **channel** , he adds.
For its 90- and 128-Mbyte, 2.5-inch glass-platter drives, Areal...

16/3,K/16 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2006 The Gale Group. All rts. reserv.

05558387 SUPPLIER NUMBER: 11667058 (USE FORMAT 7 OR 9 FOR FULL TEXT)
MIPS offers ACE/ARC system design. (MIPS Computer Systems, Advanced Computing Environment, Advanced RISC Computing)(reduced-instruction-set computing) (Most Significant Bits)
Microprocessor Report, v5, n23, p4(1)

Dec 18, 1991
ISSN: 0899-9341 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 572 LINE COUNT: 00043

... logic. One ASIC implements the address path, and another implements the data path; the data **path** ASIC is used twice. The set of **three ASICs interfaces** the R4000 to a 128-bit-wide, two-way interleaved DRAM **array** and a 64-bit-wide VRAM frame **buffer** . It also generates a 486-like bus, which interfaces to the system peripherals and connects...

16/3,K/20 (Item 6 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2006 The Gale Group. All rts. reserv.

05214804 SUPPLIER NUMBER: 11041521 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Next-generation PC designs push system performance to the limit.
Bursky, Dave
Electronic Design, v39, n12, p40(3)
June 27, 1991
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2146 LINE COUNT: 00169

... path that consists of a dual-port data path surrounding a single-port static-RAM **memory array** . Data leaving the SRAMs is stored in holding registers on both ports to accommodate the slower external bus speeds of the CPU and the system. Similarly, data entering the **memory** must be first loaded into holding registers to avoid internal bus conflicts and to ensure...

16/3,K/27 (Item 13 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2006 The Gale Group. All rts. reserv.

04824215 SUPPLIER NUMBER: 09548429 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Five years ago.
Computergram International, n1543, CGI10300019
Oct 30, 1990
ISSN: 0268-716X LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 15525 LINE COUNT: 01230

... Unisys 1100/2200 Series, V Series or A Series mainframes; the products feature eight host **channel** interfaces per **dual controller** , up to 32Gb of **disk storage** per system, a 3Mbyte-per-second transfer rate, up to 72Mb of mirrored **cache** per system with 0.5mS average access time, and up to 2.3Gb of 2...
? t16/3,k/30-31,34-35,38-39

16/3,K/30 (Item 16 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2006 The Gale Group. All rts. reserv.

03939212 SUPPLIER NUMBER: 09522811 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Three years ago.
Computergram International, n1099, CGI01130037
Jan 13, 1989
ISSN: 0268-716X LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 15822 LINE COUNT: 01257

... Unisys 1100/2200 Series, V Series or A Series mainframes; the products feature eight host **channel** interfaces per **dual controller** , up to 32Gb of **disk storage** per system, a 3Mbyte-per-second transfer rate, up to 72Mb of mirrored **cache** per system with 0.5mS average access time, and up to 2.3Gb of 2...

16/3,K/31 (Item 17 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

03915934 SUPPLIER NUMBER: 07604213 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Amperif enters Unisys-Burroughs market. (Amperif Model 8200-30 Mass Storage System) (product announcement)
Information Today, v6, n5, p54(1)
May, 1989
DOCUMENT TYPE: product announcement ISSN: 8755-6286 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 352 LINE COUNT: 00028

... necessary and it requires no additional operating system modules. Major features of the new mass **storage** system include dual access controllers, up to eight host channel interfaces per dual controller, up to 16 gigabytes of **disk** **storage** per cabinet or 32 gigabytes per system; average **disk** seek time of 16 milliseconds; a 3.0 megabyte per second **disk** transfer rate; up to 72 megabytes of mirrored **cache** per system with 0.5 millisecond average access time; and up to 2.3 gigabytes of solid state **disk** per system with an access time of 0.002 milliseconds.

16/3,K/34 (Item 1 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

02184245
AMPERIF ENTERS UNISYS/BURROUGH MARKET WITH INTEGRATED CACHE DISK STORAGE SYSTEM
News Release April 17, 1989 p. 1

... Series mainframe peripherals marketplace with the debut of an integrated fault tolerant, high performance mass **storage** system combining rotating **disk** , **cache** **disk** and solid state **disk** . **Cache** **disk** technology has been successfully implemented in the company's Unisys 1100/2200 Series-compatible mass **storage** products for more than eight years, providing increased performance improvement to Unisys 1100 and 2200 mainframes. The new Amperif Model 8200-30 is a fault tolerant implementation of this same **cache** **disk** technology, combining innovative mirrored image **cache** and nonvolatile **memory** technology. As a true fault tolerant system, the 8200-30 has no single point of failure. Mirrored image **cache** allows users to maintain two identical copies of the data in **cache** . Each mirror **cache** module has its own **memory** control, power supply and battery backup, so if there's any component failure or power...

...in one of the modules, no data is lost. Major features of the new mass **storage** system include **dual** access **controllers** , up to eight host **channel** interfaces per **dual** **controller** , up to 16 gigabytes of **disk** **storage** per cabinet or 32 gigabytes per system; average **disk** seek time of 16 milliseconds; a 3.0 megabyte per second **disk** transfer rate; up to 72 megabytes of mirrored **cache** per system with 0.5 millisecond average access time; and up to 2.3 gigabytes of solid state **disk** per system with an access time of 0.002 milliseconds.

16/3,K/35 (Item 2 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

02023062
Amperif intros Unisys storage system
MIS Week October 3, 1988 p. 14

ISSN: 0199-8838

Amperif has introduced the Amperif Model 9200 Mass **Storage** System for Unisys 1100/2200 Series computers. The new system has a **dual** access **controller** , 2-8 I/O **channel** attachments, 32 Gbytes of unformatted **disk storage** , and a semiconductor **memory** of 2.3 Gbytes for **cache disk** and/or solid state **disk** operation. The 9200 Dual **Storage** Controller has 2 separate **storage** controllers and uses the Block Multiplexor channel interface--either 4 or 8 block multiplexor channels--to connect to a Unisys 1100/2200 Series mainframe. The **storage** system's 9230 **Disk Storage** Module Cabinet contains the addressable 9235 **disk** drives with 1 Gbyte of unformatted capacity, expandable to 16 Gbytes. The 9235 Model J **Disk** Drive has a 3 Mbytes/s transfer rate, 21.3 ms of average access time...

16/3,K/38 (Item 5 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

01984743
CACHE DISK SUBSYSTEM FIRST FOR CYBER USERS
News Release July 13, 1988 p. 1

Expanding its mass **storage** system product line beyond the Unisys-compatible marketplace, Amperif Corporation has entered the Control Data peripherals market with a high performance, high capacity **cache disk** subsystem for CDC 170/180 Series mainframes. The Amperif Model 7200 represents the first CDC-compatible mass **storage** system available to Cyber Series users, featuring **dual** access **controllers** , two to eight I/O **channel** attachments, up to 17 gigabytes of **disk storage** and as much as 90 megabytes of **cache memory** . **Cache disk** technology for mainframes, pioneered by Amperif eight years ago, can significantly increase the performance of...

... eliminating the I/O bottlenecks caused by rotational latency and seek delays on conventional rotating **disk storage** . Amperif's intelligent caching scheme keeps large amounts of the most frequently used **disk** data in high speed semiconductor **memory** . Recent benchmark tests at Chrysler Corp., for example, show response time improvement of as much...

16/3,K/39 (Item 6 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

01971035
Cache disk subsystem for CDC mainframe out
MIS Week July 25, 1988 p. 11
ISSN: 0199-8838

Amperif (Chatsworth, CA) has introduced a **cache disk** subsystem for Control Data Cyber 170 and 180 Series mainframes. The new Model 7200 has **dual** access **controllers** 2-8 I/O **channel** attachments, a maximum 17 Gbytes of **disk storage** , and up to 90 Mbytes of **cache memory** . The subsystem uses the standard Cyber data channel to connect to Control Data CPUs; it...
?
PLEASE ENTER A COMMAND OR BE LOGGED OFF IN 5 MINUTES
? t16/3,k/46,49,51-52,54-56

16/3,K/46 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01469201 SUPPLIER NUMBER: 11175209 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Cubix serves a rack. (Cubix Corp. introduces LAN CentralStation 80486-based file server in rack-mount cabinet) (New products) (product announcement)
LAN Technology, v7, n9, p90(2)
Sept, 1991
DOCUMENT TYPE: product announcement ISSN: 1042-4695 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 356 LINE COUNT: 00026

... 33-MHz 80486 CPU, 4 Mbytes of RAM (expandable to 64 Mbytes), 256 Kbytes of **cache** , and an EISA bus. The file server sits in a drawer with room for two hard drives and one 5.25- and one 3.5-inch floppy drive. A multi- **channel** I/O board gives the file server **two** COM **ports** , an LPT port, a floppy **disk** controller, and keyboard support. An optional drive subsystem contains mounting for eight half-height or four full-height Maxtor Corp. drives. Depending on drive capacity choices, total **storage** can reach 10 Gbytes.
LAN Central-Station's gateway subsystem offers a 12-slot segmented...

16/3,K/49 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01417205 SUPPLIER NUMBER: 10368717 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Banyan certifies two EISA servers for VINES. (Banyan Systems Inc. certifies file servers from Advanced Logic Research and Tricord Systems for its network operating system)
Buckler, Grant
Newsbytes, NEW02150011
Feb 15, 1991
LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 284 LINE COUNT: 00023

... the Extended Industry Standard Architecture (EISA) bus, the units incorporate a scalable read/write-back **cache** **memory** architecture and **dual** - **processor** upgrade **path** to accommodate two 33-MHz 486 microprocessors and up to a megabyte of ALR ProCache **memory** on one 12-slot system board.
Tricord's PowerFrame servers were designed for local area...

16/3,K/51 (Item 6 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2006 The Gale Group. All rts. reserv.

01319749 SUPPLIER NUMBER: 07993458 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Multiprotocol processor marries 68000 and RISC. (Motorola's MC68302 Integrated Multiprotocol Processor includes reduced-instruction-set computer controller)
Miller, Arthur R.
ESD: The Electronic System Design Magazine, v19, n11, p65(3)
Nov, 1989
ISSN: 0893-2565 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2102 LINE COUNT: 00167

... functionality for data-only terminals. A RISC controller manages a buffer structure for the serial **channels** and reduces total serial **channel** size. A **dual** - **port** **memory** isolates the serial **channels** from the 68000 processor core. DMA was added for the serial channels to support flexible location of data **buffers** throughout the processor or user **memory** map, while freeing the 68000 processor to perform other tasks. Also available is a general...

16/3,K/52 (Item 7 from file: 275)

DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2006 The Gale Group. All rts. reserv.

01317685 SUPPLIER NUMBER: 07947916 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Z80 communications controller chip cuts execution time to 300ns. (Hitachi HD64180S) (product announcement)
Wilson, Ron
Computer Design, v28, n21, p110(1)
Nov 1, 1989
DOCUMENT TYPE: product announcement ISSN: 0010-4566 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 640 LINE COUNT: 00051

... a rather sophisticated DMA controller with features that are tuned to the communications environment. The **dual - channel controller** provides for **memory** -to- **memory** , **memory** -to-I/O and **memory** -to-serial-interface transfers. When working with the primary serial interface, the DMA controller can operate in a chained mode, moving data between the interface and scattered **buffers** without any CPU intervention.
The primary peripheral modules on the 64180S are, of course, the...

16/3,K/54 (Item 9 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2006 The Gale Group. All rts. reserv.

01291345 SUPPLIER NUMBER: 07134548 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Minigrams.
Computergram International, n1143, pELECTRNC ED
March 24, 1989
LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 2169 LINE COUNT: 00167

... Looking to the 1992 European Single Market, the Chatsworth, California manufacturer of Unisys compatible mass **storage** systems and relational database management systems, Amperif Corp is to set up a sales and...

...but it has not said where it will be: Amperif offers fault tolerant, mirror image **cache** **disk** systems with its new 8200 and 9200 mass **storage** systems, which it claims enhance the performance of Unisys 1100/2200 Series, V Series or A Series mainframes; the products feature eight host **channel** interfaces per **dual** **controller** , up to 32Gb of **disk** **storage** per system, a 3Mbyte-per-second transfer rate, up to 72Mb of mirrored **cache** per system with 0.5mS average access time, and up to 2.3Gb of 2...

16/3,K/55 (Item 10 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2006 The Gale Group. All rts. reserv.

01261013 SUPPLIER NUMBER: 07223353 (USE FORMAT 7 OR 9 FOR FULL TEXT)
The Next architecture: design for the '90s?
Williams, Tom
Computer Design, v27, n22, p27(2)
Dec, 1988
ISSN: 0010-4566 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1491 LINE COUNT: 00116

... computer, however, lies in its intelligent I/O processing. Recognizing that contention among peripherals for **memory** bandwidth represents a bottleneck in terms of both the **memory** bus and CPU time, Next has implemented two VLSI application-specific IC chips that it...

...that the system takes advantage of a technique long used in mainframes of dedicating intelligent **channel** processors to each I/O **channel** .
These **two** **ASICs** are the integrated **channel** processor (ICP) and the optical **storage** processor (OSP). The ICP provides 12 separate, buffered DMA channels to manage all system I...

...these channels, for example, are dedicated to the on-board Ethernet networking interface. The channels **buffer** data coming from Ethernet and send it to **memory** in 128-bit burst mode rather than in 32-bit chunks, thus taking a burden off **memory** .
The ICP supports other DMA channels: to the monitor, the printer, serial ports (two channels...

16/3,K/56 (Item 11 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01251233 SUPPLIER NUMBER: 06835939 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Disk array features 1-Gbyte fault-tolerant storage.
Williams, Tom
Computer Design, v27, n12, p33(1)
June 15, 1988
ISSN: 0010-4566 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 720 LINE COUNT: 00054

... a result of the fault-tolerant measures, which also include redundant power supplies and data **paths** .
Dual 80386 **processors**
The **storage** subsystem incorporates **dual** 80386 **processors** or arbitrate among different hosts by preventing simultaneous access to the same files. The dual...

...and provide equal-priority access to all hosts. In addition, the procesors manage a subsystem **cache** **memory** of up to 8 Mbytes and support overlapped seeks, a SCSI capability that lets a...
? t16/3,k/66

16/3,K/66 (Item 5 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

01089594 Supplier Number: 40729844 (USE FORMAT 7 FOR FULLTEXT)
AMPERIF TO SET UP SUPPORT ORGANISATION BASED WITHIN THE EC
Computergram International, n1143, pN/A
March 28, 1989
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 147

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
Looking to the 1992 European Single Market, the Chatsworth, California manufacturer of Unisys compatible mass **storage** systems and relational database management systems, Amperif Corp is to set up a sales and...

...but it has not said where it will be: Amperif offers fault tolerant, mirror image **cache** **disk** systems with its new 8200 and 9200 mass **storage** systems, which it claims enhance the performance of Unisys 1100/2200 Series, V Series or A Series mainframes; the products feature eight host **channel** interfaces per **dual** **controller** , up to 32Gb of **disk** **storage** per system, a 3Mbyte-per-second transfer rate, up to 72Mb of mirrored **cache** per system with 0.5mS average access time, and up to 2.3Gb of 2...
?

```
File   2:INSPEC 1898-2006/Oct W4
         (c) 2006 Institution of Electrical Engineers
File   6:NTIS 1964-2006/Oct W4
         (c) 2006 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2006/Oct W4
         (c) 2006 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2006/Oct W4
         (c) 2006 The Thomson Corp
File  35:Dissertation Abs Online 1861-2006/Oct
         (c) 2006 ProQuest Info&Learning
File  65:Inside Conferences 1993-2006/Nov 01
         (c) 2006 BLDSC all rts. reserv.
File  94:JICST-EPlus 1985-2006/Jul W3
         (c)2006 Japan Science and Tech Corp(JST)
File  95:TEME-Technology & Management 1989-2006/Oct W5
         (c) 2006 FIZ TECHNIK
File  99:Wilson Appl. Sci & Tech Abs 1983-2006/Sep
         (c) 2006 The HW Wilson Co.
File 144:Pascal 1973-2006/Oct W2
         (c) 2006 INIST/CNRS
File 256:TecInfoSource 82-2006/Apr
         (c) 2006 Info.Sources Inc
File 266:FEDRIP 2006/Aug
         Comp & dist by NTIS, Intl Copyright All Rights Res
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 2006 The Thomson Corp
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group

Set     Items   Description
S1     324012   CACHE? ? OR SUBCACH? OR MICROCACH? OR BUFFER? ? OR SUBBUFF-
              ER? OR MICROBUFFER?
S2     715188   DISK? ? OR DISKETTE? OR DISC? ? OR DISCETTE? OR DISKDRIVE?
              OR DISCDRIVE? OR DISKARRAY? OR DISCARRAY? OR TAPEDRIVE? OR TA-
              PE? ?
S3    1616357   MEMORY? OR STORAGE?
S4    9829889   CONTROL???? OR MICROCONTROL? OR INTERFACE? ? OR PORT? ? OR
              ASIC? ? OR PROCESS?R? ? OR MICROPROCESS?
S5    1065229   ICC OR ICCS OR IC OR ICS OR (INTEGRATED OR MICRO)(1W)CIRCU-
              IT? ? OR CKT? ? OR MICROCIRCUIT? OR MICROCHIP? ? OR CHIP? ? OR
               SILICONCHIP?
S6    1892444   COMPUTERCHIP? OR SOC OR SEMICOND? ? OR SEMICONDUCT?R? ? OR
              SEMI()(COND? ? OR CONDUCT?R? ?)
S7     132103   (PLURALITY OR MULTIPLE OR MANY OR MULTI OR SEVERAL OR ADDI-
              TIONAL OR DIFFERENT OR SECOND OR 2ND OR NUMBER OR ALTERNATIVE-
              )(1W)S4:S6
S8     146958   (PAIR OR EXTRA OR ANOTHER OR SECONDARY OR DUAL OR THREE OR
              TWO OR PARALLEL OR REDUNDANT OR ALTERNATE OR COUPLE)(1W)S4:S6
S9       1902   (THIRD OR 3RD)(1W)S4:S6
S10   3207743   PATH? ? OR DATAPATH? OR PATHWAY? OR ROUTE OR ROUTES OR CHA-
              NNEL? ?
S11      3889   S7:S9(7N)S10
S12       158   S11 AND S1
S13        89   S12 AND S2:S3
S14        21   S12 AND ARRAY? ?
S15        90   S13:S14
S16        70   S15/1992:2006
S17        20   S15 NOT S16
S18        15   RD  (unique items)

 18/7/1     (Item 1 from file: 2)
DIALOG(R)File   2:INSPEC
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05012087 INSPEC Abstract Number: C91072609
Title: Cache coherence in systems with parallel communication channels and many processors
Author(s): Willis, J.C.; Sanderson, A.C.; Hill, C.R.
Author Affiliation: Philips Lab., Briarcliff Manor, NY, USA
Conference Title: Proceedings of Supercomputing '90 (Cat. No.90CH2916-5) p.554-63
Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA
Publication Date: 1990 Country of Publication: USA xxv+982 pp.
ISBN: 0 8186 2056 0
U.S. Copyright Clearance Center Code: CH2916-5/90/0000-0554$01.00
Conference Sponsor: IEEE; ACM; Lawrence Livermore Nat. Lab.; Los Alamos Nat. Lab.; NASA Ames Res. Center; Nat. Center Atmos. Res.; NSF; SIAM; Supercomput. Res. Center
Conference Date: 12-16 Nov. 1990 Conference Location: New York, NY, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: The authors describe and analyze two algorithms for maintaining cache coherence in multiprocessor systems with parallel communication channels and many processors . A distributed link-list relates all cache frames representing the same main memory block. Messages traverse the list to maintain list integrity, exclusive ownership, and consistent values. Memory access semantics are equivalent to a shared memory system without caches . Reference latency, efficiency of memory use, and hardware complexity are moderate and well-bounded. A brief comparison with the Scalable Coherent Interface illustrates some of the design tradeoffs associated with distributed directory algorithms. (12 Refs)
Subfile: C

18/7/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

04186073 INSPEC Abstract Number: C88045617
Title: The Amperif Cache Disk System
Author(s): Fuld, S.
Conference Title: Digest of Papers: COMPCON Spring 88. Thirty-Third IEEE Computer Society International Conference (Cat. No.88CH2539-5) p.156-7
Publisher: IEEE Comput. Soc. Press, Washington, DC, USA
Publication Date: 1988 Country of Publication: USA xvi+549 pp.
ISBN: 0 8186 0828 5
U.S. Copyright Clearance Center Code: CH2539-5/88/0000-0156$01.00
Conference Sponsor: IEEE
Conference Date: 29 Feb.-3 March 1988 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: A description is given of the Amperif Cache Disk System, which provides high performance, large capacity, very flexible, low cost ownership storage for users of a variety of mainframe CPUs. High-speed logic combined with full read and write, track-oriented cache , multiple - channel ports , and data paths as well as disk array design give a high-performance level. The modular architecture of the system provides flexibility for a variety of host interfaces, storage configurations, and operating modes. The system uses a fraction of the floor space, power, and air conditioning of comparable products. Due care was taken to assure data integrity throughout the system. (0 Refs)
Subfile: C

18/7/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

04150536 INSPEC Abstract Number: B88039621
Title: VLSI memory management for an eight Gigabit/s memory system
Author(s): Fernandez, A.; Jaquez, M.; Robbins, J.
Author Affiliation: Bell Commun. Res., Appl. Res. Labs., Morristown, NJ, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering vol.845 p.345-9
Publication Date: 1987 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
Conference Title: Visual Communications and Image Processing II
Conference Sponsor: SPIE
Conference Date: 27-29 Oct. 1987 Conference Location: Cambridge, MA, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Practical (P)
Abstract: Describes two ASIC devices which are the building blocks for the memory management of an 8 Megabyte video memory system. The devices are used in tandem to synchronize, buffer , multiplex, and execute 256 million 4 byte I/O requests per second for a total transfer capacity of 8 Gigabits per second. Requests are communicated to the memory over 16 asynchronous channels. The first device, the memory channel interface (MCI), synchronizes, buffers , and routes incoming address, data, and control bits from the input/output channels to the second ASIC device, the memory module interface (MMI). The MMI device interfaces the MCI with static memory chips, and produces the proper control signals for the memory 's operation. The MCI and MMI devices allow the high performance video memory to be realized with approximately 150 devices. (2 Refs)
Subfile: B

18/7/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

03702569 INSPEC Abstract Number: C86038910
Title: A new computing system-the JSEP-ES 1046
Author(s): Weichet, P.; Neuwirth, P.
Journal: Vyber Informaci z Organizacni a Vypocetni Techniky no.1 p. 3-13
Publication Date: 1986 Country of Publication: Czechoslovakia
CODEN: VIOTDB ISSN: 0322-8681
Language: Czech Document Type: Journal Paper (JP)
Treatment: Practical (P); Product Review (R)
Abstract: Describes the hardware and software of the JSEP-ES 1046 general-purpose computer made in the Soviet Union. The ES 1046 is program compatible with the JSEP1, JSEP2 and JSEP3 computers. It features semiconductor memory with the capacity of 4 Mbytes, reading access time below 550 ns, memory cycle time below 700 ns and input power below 1.8 kVA; fast buffer memory with the capacity of 16 KBytes; and six multiple channels. Optional features include matrix processor facilities for providing two - processor architecture and three channel - channel adapters. Remote maintenance facilities are also available. Eleven configurations of the ES 1046 will be available, five of these with peripherals and six without. The system software consists of a complex of OS-7/ES operating systems and a system of diagnostic programs including complex automatic testing facilities. (0 Refs)
Subfile: C

18/7/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

03158597 INSPEC Abstract Number: B83063141, C84002135
Title: Monolithic 8 channel analog to digital converter with onboard memory
Author(s): Wynne, J.; Travers, D.
Conference Title: Southcon/81 Conference Record p.18-3/1-5
Publisher: Electron. Conventions, El Segundo, CA, USA
Publication Date: 1981 Country of Publication: USA 760 pp.
Conference Date: 13-15 Jan. 1981 Conference Location: Atlanta, GA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Discusses a single chip CMOS 8 channel data acquisition system which includes a dual port memory operated in the Direct Memory Access mode. The memory serves as a data buffer between the A/D converter and the microcomputer. The microcomputer treats the dual port memory as part of its assigned memory space and obtains the value of an analog input by reading the memory as it would for any conventional memory location. (0 Refs)
Subfile: B C

18/7/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

02615079 INSPEC Abstract Number: C81002137
Title: DAS packs memory for easy mu P interface
Author(s): Tucholski, H.
Author Affiliation: Analog Devices Inc., Norwood, MA, USA
Journal: Electronic Design vol.28, no.19 p.79-83
Publication Date: 13 Sept. 1980 Country of Publication: USA
CODEN: ELODAW ISSN: 0013-4872
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Presents a microprocessor-compatible data-acquisition IC which eliminates the need to wait for a-d conversion data. The AD7581 from Analog Devices contains dual - port , 8-byte RAM, an eight- channel multiplexer, an 8-bit successive-approximation a-d converter, address latches, interface logic, and three-state buffers for direct connection to a microprocessor .bus-all on a single 147*125-mil CMOS chip. With all conveniences, including memory , right on board, there is no need for interrupt software, and data are simply taken from the a-d converter in a normal microprocessor data-read cycle. The AD7581 can be treated by a microprocessor as a fast memory , which makes interfacing to processors relatively easy. (0 Refs)
Subfile: C

18/7/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

0000750163 INSPEC Abstract Number: 1965B17370
Title: Transmission capacity of disk storage systems with concurrent arm positioning
Author(s): Fife, D.W.; Smith, J.L.
Journal: IEEE Transactions on Electronic Computers EC-14 4 p. 575-582
Publication Date: Aug. 1965 Country of Publication: USA
Language: English Document Type: Journal Paper (JP)
Abstract: An organization for a disk storage system oriented toward multicomputer and shared computer applications is described, and a study is made of its effectiveness in accessing data. The disk file incorporates an independently positioned arm for accessing each disk , and the capability for concurrently controlling several positioners. Also, multiple data transmission channels can be provided between the disk file and a

buffer unit. A criterion of maximum average transmission capacity is proposed for investigating the speed of accessing data with this organization. Probabilistic models for analysing the queueing of positioned arms for access to a **disk - buffer** transmission channel are developed. With reasonable assumptions, the solution of the models is reduced to a small set of linear equations in terms of queue length probabilities. The transmission capacity is evaluated with parameter values typical of contemporary **disk** files. The principal conclusion is that the economic feasibility of more than **three** position **controllers** per **disk - buffer** **channel** is very doubtful in seeking the full effectiveness of this organization.
Subfile: B C

18/7/9 **(Item 1 from file: 6)**
DIALOG(R)File 6:NTIS

1218766 NTIS Accession Number: AD-D011 968/5
Interactive Communication Channel
(Patent)
Chan, R. H. ; Mann, M. R. ; Ciarrocchi, J. A.
Department of the Air Force, Washington, DC.
Corp. Source Codes: 000260000; 109850
Report No.: PAT-APPL-6-686 954; PATENT-4 546 429
Filed 27 Dec 84 patented 8 Oct 85 30p
Languages: English Document Type: Patent
Journal Announcement: GRAI8606
Supersedes PAT-APPL-6-686 954, AD-D011 580.
This Government-owned invention available for U.S. licensing and, possibly, for foreign licensing. Copy of patent available Commissioner of Patents, Washington, DC 20231 $1.00.
NTIS Prices: Not available NTIS
Country of Publication: United States
This patent discusses an interactive communications channel (ICC) for providing a digital computer with high-performance **multi - channel** **interfaces** . Sixteen full duplex **channels** can be serviced in the ICC with the sequence or scan pattern being programmable and dependent upon the number of channels and their speed. A channel **buffer** system is used for line interface, and character exchange. The channel **buffer** system is on a byte basis. The ICC performs frame start and frame end functions, bit stripping and bit stuffing. Data is stored in a **memory** in block format (256 bytes maximum) by a program control and the ICC maintains byte address information and a block byte count. Data exchange with a **memory** is made by cycle steals. Error detection is also provided for using a cyclic redundnacy check technique.
? t18/7/11-12,15

18/7/11 **(Item 3 from file: 6)**
DIALOG(R)File 6:NTIS

0603357 NTIS Accession Number: AD-A034 658/5/XAB
Associative Processor I/O Design and Specification
(Final technical rept. 9 Apr-9 Aug 76)
Kroeger, M. J.
Goodyear Aerospace Corp Akron Ohio
Corp. Source Codes: 156800
Report No.: GER-16378; RADC-TR-76-352
Nov 76 49p
Journal Announcement: GRAI7707
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road,

Springfield, VA, 22161, USA.
NTIS Prices: PC A03/MF A01
Contract No.: F30602-76-C-0240; 5597; 14
Detailed input/output (I/O) specifications were compiled for the three interface channels that currently exist in the STARAN associative processing computer at RADC: (1) buffered I/O (BIO), (2) direct memory access (DMA), and (3) external function (EXF). The availability and location of port connections for these channels are included within the I/O specifications. A comprehensive philosophy was developed that provides an interface between various external devices and the parallel input/output PIO unit. The recommended PIO expansion method uses a daisy-chain approach, where each external device is constrained to repeat all the signal of the PIO channel. The expansion method contains a control channel and four 256-bit-wide data ports. These data ports connect external devices to the PIO unit. The associative arrays also connect to the PIO unit through four existing ports. Since the associative array ports contain intermediate buffer registers, the recommended expansion data ports are not buffered. To minimize the number of cable wires and signal repeaters, the PIO expansion approach uses bi-directional lines and time-multiplexed data transmission. In this way, 32 lines are used to transmit a 256-bit-data word in either direction. A detailed logic design of the recommended PIO expansion philosophy was completed; three new PC boards were designed as part of this effort. (Author)

18/7/12 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02687965 E.I. Monthly No: EIM8812-061107
Title: WISCONSIN MULTICUBE: A NEW LARGE-SCALE CACHE -COHERENT MULTIPROCESSOR.
Author: Goodman, James R.; Woest, Philip J.
Corporate Source: Univ of Wisconsin, Madison, WI, USA
Conference Title: 15th Annual International Symposium on Computer Architecture, Conference Proceedings.
Conference Location: Honolulu, HI, USA Conference Date: 19880530
Sponsor: IEEE Computer Soc, Technical Committee on Computer Architecture, Los Alamitos, CA, USA; ACM, Dearborn, MI, USA; IEEE, New York, NY, USA
E.I. Conference No.: 11737
Source: Publ by IEEE, New York, NY, USA. Available from IEEE Service Cent (Cat n 88CH2545-2), Piscataway, NJ, USA p 422-431
Publication Year: 1988
ISBN: 0-8186-0861-7
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8812
Abstract: The Wisconsin multicube, a large-scale, shared- memory multiprocessor architecture that uses a snooping cache protocol over a grid of buses, is introduced. Each processor has a conventional (SRAM) cache optimized to minimize latency and a large (DRAM) snooping cache optimized to reduce bus traffic and to maintain consistency. The large snooping cache should guarantee that nearly all the traffic on the buses will be generated by I/O and accesses to shared data. The programmer's view of the system is like a multi, a set of processors having access to a common shared memory with no notion of geographical locality. Thus writing software, including the operating system, should be a straightforward extension of those techniques being developed for multis. The interconnection topology allows for a cache -coherent protocol for which most bus requests can be satisfied with no more than twice the number of bus operations required for a single-bus multi. The total symmetry guarantees that there are no topology-induced bottlenecks. The total bus bandwidth grows in proportion to the product of the number of processors and the average path length. The proposed architecture is an example of a novel class of interconnection topologies - the multicube - which

consists of N equals n**k processors, where each processor is connected to k buses and each bus is connected to n processors. 15 refs.

18/7/15 (Item 1 from file: 583)

03824144
ADVANCED LOGIC AIMS TO CRUSH COMPAQ WITH POWER
US - ADVANCED LOGIC AIMS TO CRUSH COMPAQ WITH POWER
Computergram International (CGI) 8 November 1990 p1
ISSN: 0268-716X

Advanced Logic Research (Irvine, CA) has introduced its new family of 33MHz 80486-based servers Powerpro, intended to follow Compaq Computer's Systempro. The EISA bus machines offer a scalable **cache** and **dual processor** upgrade **path** to accommodate two of the processors and up to 1Mb of Server **Cache** on a single 12-slot system board. There is room for 49Mb on the system board, and the company claims performance of 14.7 to 40 MIPS, and it supports the Santa Cruz Operation SCO Unix System V.386 3.2 with MPX multiprocessor extensions. It also runs NetWare 386 and offers **disk** mirroring, duplexing and spanning. Prices go from USDlr7,500 to USDlr25k, ships first quarter 1991.*
?

File 696:DIALOG Telecom. Newsletters 1995-2006/Oct 31
(c) 2006 Dialog
File 15:ABI/Inform(R) 1971-2006/Oct 31
(c) 2006 ProQuest Info&Learning
File 98:General Sci Abs 1984-2006/Oct
(c) 2006 The HW Wilson Co.
File 112:UBM Industry News 1998-2004/Jan 27
(c) 2004 United Business Media
File 141:Readers Guide 1983-2006/Aug
(c) 2006 The HW Wilson Co
File 484:Periodical Abs Plustext 1986-2006/Oct W4
(c) 2006 ProQuest
File 813:PR Newswire 1987-1999/Apr 30
(c) 1999 PR Newswire Association Inc
File 635:Business Dateline(R) 1985-2006/Oct 31
(c) 2006 ProQuest Info&Learning
File 810:Business Wire 1986-1999/Feb 28
(c) 1999 Business Wire
File 369:New Scientist 1994-2006/Aug W4
(c) 2006 Reed Business Information Ltd.
File 370:Science 1996-1999/Jul W3
(c) 1999 AAAS
File 674:Computer News Fulltext 1989-2006/Sep W1
(c) 2006 IDG Communications
File 647:CMP Computer Fulltext 1988-2006/Dec W3
(c) 2006 CMP Media, LLC

Set	Items	Description
S1	101319	CACHE? ? OR SUBCACH? OR MICROCACH? OR BUFFER? ? OR SUBBUFFER? OR MICROBUFFER?
S2	492078	DISK? ? OR DISKETTE? OR DISC? ? OR DISCETTE? OR DISKDRIVE? OR DISCDRIVE? OR DISKARRAY? OR DISCARRAY? OR TAPEDRIVE? OR TAPE? ?
S3	623047	MEMORY? OR STORAGE?
S4	2643652	CONTROL???? OR MICROCONTROL? OR INTERFACE? ? OR PORT? ? OR ASIC? ? OR PROCESS?R? ? OR MICROPROCESS?
S5	384627	ICC OR ICCS OR IC OR ICS OR (INTEGRATED OR MICRO)(1W)CIRCUIT? ? OR CKT? ? OR MICROCIRCUIT? OR MICROCHIP? ? OR CHIP? ? OR SILICONCHIP?
S6	226619	COMPUTERCHIP? OR SOC OR SEMICOND? ? OR SEMICONDUCT?R? ? OR SEMI()(COND? ? OR CONDUCT?R? ?)
S7	52627	(PLURALITY OR MULTIPLE OR MANY OR MULTI OR SEVERAL OR ADDITIONAL OR DIFFERENT OR SECOND OR 2ND OR NUMBER OR ALTERNATIVE-)(1W)S4:S6
S8	63820	(PAIR OR EXTRA OR ANOTHER OR SECONDARY OR DUAL OR THREE OR TWO OR PARALLEL OR REDUNDANT OR ALTERNATE OR COUPLE)(1W)S4:S6
S9	3087	(THIRD OR 3RD)(1W)S4:S6
S10	1209811	PATH? ? OR DATAPATH? OR PATHWAY? OR ROUTE OR ROUTES OR CHANNEL? ?
S11	2275	S7:S9(7N)S10
S12	107	S11(S)S1
S13	69	S12(S)(S2:S3 OR ARRAY? ?)
S14	55	S13/1992:2006
S15	14	S13 NOT S14
S16	13	RD (unique items)

16/3,K/1 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00444805 89-16592
MPH - A Hybrid Parallel Machine
Fernandes, E. S. T.; de Amorim, C. L.; Barbosa, V. C.; Franca, F. M. G.; de Souza, A. F.
Microprocessing & Microprogramming v25n1-5 PP: 229-232 Jan 1989

ISSN: 0165-6074 JRNL CODE: EUJ

...ABSTRACT: point communication links - the usual approach in connecting pairs of neighboring nodes in a hypercube - **memory** segments that are shared by each **pair** of **processors** are chosen for the realization of communication **channels** in the architecture. In addition to the use of message passing **buffers** , the shared **memory** segments can store shared data and code segments. These characteristics make MPH a hybrid machine.

16/3,K/2 (Item 2 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00389141 88-05974
Better Bus Designs
Cook, Rick
Computer & Communications Decisions v20n1 PP: 41-43 Jan 1988
ISSN: 0010-4558 JRNL CODE: COM

...ABSTRACT: of the new buses are matching bus speed or bandwidth more closely with processor and **memory** speed and the management of specialized processors. The IBM Corp. Micro Channel and the Apple Computer Inc. Nu Bus offer improvements in both areas. Although it can support **multiple processors** , Micro **Channel** may bog down with two 32-bit processors. Unlike Micro Channel, Apple's Nu Bus...

...a multimaster design but addresses the most serious performance bottleneck with a separate, high-speed **memory** -to-processor bus and a **memory** **cache** to reduce bus traffic. With Smartslot, AST Research Inc. provides compatibility with the IBM PC...

16/3,K/3 (Item 1 from file: 141)
DIALOG(R)File 141:Readers Guide

01281572 H.W. WILSON RECORD NUMBER: BRGA88031572
Motorola pushing 88000 as chip of the nineties.
Byte (Byte) v. 13 (June '88) p. 12+
LANGUAGE: English

...ABSTRACT: with separate address and data lines for a program's code and data. These dual **paths** improve throughput. The 88000 comprises **three** **chips** : the MC88000 central processor and two MC88200 **cache / memory** management units that oversee the code and data paths. The central processor has built-in...

16/3,K/5 (Item 1 from file: 635)
DIALOG(R)File 635:Business Dateline(R)

0246357 91-70304
ALR Challenges IBM With the Introduction of POWERPRO/MC: World's First Upgradeable Dual Processor-Ready 50-MHz i486DX Micro Channel PC on Market Today
Kirkey, Dave; Robertson, Laura
Business Wire (San Francisco, CA, US) s1 p1
PUBL DATE: 911021
WORD COUNT: 857
DATELINE: Irvine, CA, US

TEXT:

...adapt in the future. The POWERPRO/MC will deliver future performance growth by providing a **dual processor** CPU upgrade **path** . Additionally in Q2'92, ALR will offer as an option for the POWERPRO/MC, the ALR Advanced **Disk Array** (ADA) subsystem. The ALR Advanced **Disk Array** controller is a 32-bit deferred write **disk array** controller which supports **disk** mirroring, **disk** striping and **disk** spanning for maximum data security in mission-critical environments. The ALR ADA controller comes standard with 2 MB of **memory cache** expandable to 8-MB **cache** and can support an internal **disk array** of over 2 gigabytes. Equipped with the ALR Advanced **Disk Array** subsystem and a 32-bit Micro Channel bus, the POWERPRO/MC series provides the highest...

16/3,K/6 (Item 2 from file: 635)
DIALOG(R)File 635:Business Dateline(R)

0240006 91-63897
Los Alamos Licenses Supercomputer Image Device
Danneskiold, Jim
Business Wire (San Francisco, CA, US) s1 p1
PUBL DATE: 910919
WORD COUNT: 1,009
DATELINE: Los Alamos, NM, US

TEXT:

...granted Input Output Systems Corp. of Mountain View an exclusive license to manufacture a frame **buffer** . The instrument allows supercomputers equipped with the High-Performance **Parallel Interface** (HIPPI) **channel** to display movies at either 15 or 60 frames a second by consecutively writing the data that produces individual frames to one of the **buffer** 's two parallel **memory** banks.

Wally St. John of the Computer Network Engineering Group at Los Alamos developed the...

16/3,K/8 (Item 4 from file: 635)
DIALOG(R)File 635:Business Dateline(R)

0192492 91-13866
ALR's POWERPRO Dual Processor Systems First Compatible to Be Awarded Certification as Banyan VINES SMP Servers
Kirkey, Dave; Robertson, Laura
Business Wire (San Francisco, CA, US) s1 p1
PUBL DATE: 910205
WORD COUNT: 427
DATELINE: Irvine, CA, US

TEXT:

...MHz i486 and EISA-bus, the new product families incorporate a scalable read/write-back **cache memory** architecture and **dual processor** upgrade **path** to accommodate two 33-MHz i486 microprocessors and up to 1-MB of ALR ProCache...

16/3,K/9 (Item 5 from file: 635)
DIALOG(R)File 635:Business Dateline(R)

0124279 90-06949
Western Digital Announces New LAN Adapters Based on 10BaseT Draft 9

Orban, Lynda; Lahtela, Alice
Business Wire (San Francisco, CA, US) s1 p1
PUBL DATE: 900129
WORD COUNT: 747
DATELINE: Irvine, CA, US

TEXT:

...WD8003W/A) operates in all Micro Channel-bus systems and features a 16K dual port **buffer memory** for high packet throughput and the same boot ROM option (boot ROMs are available for...

16/3,K/12 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2006 CMP Media, LLC. All rts. reserv.

00643845 CMP ACCESSION NUMBER: UNX19890612S0710
Products: SysAdmin Release 3.2.2 and JobAcct Release 1.1., system administration utilities packages.... (PRODUCT BRIEFS)
UNIX TODAY , 1989, n 021, 23
PUBLICATION DATE: 890612
JOURNAL CODE: UNX LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: PRODUCTS
WORD COUNT: 2108

... order.
Profile: MicroTech says this line of controllers is designed to connect any 9-track **tape** drive to any PC or compatible system. MicroTech software is available for a variety of **tape** conversions and includes a **tape** backup/restore program. Software runs under Unix, Xenix and MS-DOS. The **TAPE** -AT 9-track **tape** controller card connects a "Pertec standard" 9-track **tape** transport to a PC or PS/2 system. Device drivers are supplied by MicroTech for...

...1 byte to infinity, data transfer rates up to 1.2 Mbps, interrupt selection of **channel** 3 through 15 and on-board " **dual port** " **buffer memory** -either 256k bytes or 1 Mbyte-according to MicroTech.Circle Reader Service No. 209
Product...

16/3,K/13 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2006 CMP Media, LLC. All rts. reserv.

00612454 CMP ACCESSION NUMBER: EBN19881024S1350
NEW PRODUCTS (621)
ELECTRONIC BUYERS' NEWS, 1988, n 621, 40
PUBLICATION DATE: 881024
JOURNAL CODE: EBN LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: 621PG40
WORD COUNT: 789

... incorporates high-performance **disk**, cache **disk** and solid-state **disk** sybsystems.
The Model 9200 mass **storage** system is a plug-compatible, high-capacity system designed for Unisys Corp. 1100/2200 Series users that allows users to access any combination of high-speed **disk** , **cache disk** and solid-state **disk** . The 9200 features a **dual** access **controller** , two to eight I/O **channel** attachments, up to 32 gigabytes of unformatted **disk storage** and up to 2.3 gigabytes of semiconductor **memory** for **cache disk** and/or solid-state **disk** operation.

The major components included in the mass storage system are the 9200 dual storage...
?

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File 348:EUROPEAN PATENTS 1978-2006/ 200643
         (c) 2006 European Patent Office
File 349:PCT FULLTEXT 1979-2006/UB=20061026UT=20061019
         (c) 2006 WIPO/Thomson

Set     Items   Description
S1     316062   CACHE? ? OR SUBCACH? OR MICROCACH? OR BUFFER? ? OR SUBBUFF-
             ER? OR MICROBUFFER?
S2     425333   DISK? ? OR DISKETTE? OR DISC? ? OR DISCETTE? OR DISKDRIVE?
             OR DISCDRIVE? OR DISKARRAY? OR DISCARRAY? OR TAPEDRIVE? OR TA-
             PE? ?
S3     609062   MEMORY? OR STORAGE?
S4    1547926   CONTROL???? OR MICROCONTROL? OR INTERFACE? ? OR PORT? ? OR
             ASIC? ? OR PROCESS?R? ? OR MICROPROCESS?
S5     371217   ICC OR ICCS OR IC OR ICS OR (INTEGRATED OR MICRO)(1W)CIRCU-
             IT? ? OR CKT? ? OR MICROCIRCUIT? OR MICROCHIP? ? OR CHIP? ? OR
              SILICONCHIP?
S6     265025   COMPUTERCHIP? OR SOC OR SEMICOND? ? OR SEMICONDUCT?R? ? OR
             SEMI()(COND? ? OR CONDUCT?R? ?)
S7     164695   (PLURALITY OR MULTIPLE OR MANY OR MULTI OR SEVERAL OR ADDI-
             TIONAL OR DIFFERENT OR SECOND OR 2ND OR NUMBER OR ALTERNATIVE-
             )(1W)S4:S6
S8     108900   (PAIR OR EXTRA OR ANOTHER OR SECONDARY OR DUAL OR THREE OR
             TWO OR PARALLEL OR REDUNDANT OR ALTERNATE OR COUPLE)(1W)S4:S6
S9      16301   (THIRD OR 3RD)(1W)S4:S6
S10    816694   PATH? ? OR DATAPATH? OR PATHWAY? OR ROUTE OR ROUTES OR CHA-
             NNEL? ?
S11     13184   S7:S9(7N)S10
S12       461   S11(25N)S1
S13       215   S12(25N)(S2:S3 OR ARRAY? ?)
S14        60   S13 AND AC=US/PR AND AY=(1963:1991)/PR
S15        60   S13 AND AC=US AND AY=1963:1991
S16        60   S13 AND AC=US AND AY=(1963:1991)/PR
S17        60   S13 AND PY=1963:1991
S18        70   S14:S17
S19        70   IDPAT (sorted in duplicate/non-duplicate order)
S20        65   IDPAT (primary/non-duplicate records only)
S21        43   S20 AND S2:S3/TI,AB
S22        80   S12(25N)(STORAGE? OR ARRAY? ?)
S23        19   S22 AND AC=US/PR AND AY=(1963:1991)/PR
S24        19   S22 AND AC=US AND AY=1963:1991
S25        19   S22 AND AC=US AND AY=(1963:1991)/PR
S26        21   S22 AND PY=1963:1991
S27        21   S23:S26
S28        21   IDPAT (sorted in duplicate/non-duplicate order)
S29        20   IDPAT (primary/non-duplicate records only)
?
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? t21/5,k/19

21/5,K/19 (Item 19 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00341729
Cache storage **system.**
Cache-Speicheranordnung.
Systeme d'antememoire.
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Gallagher, Patrick Wayne, 141 Melbourne Street, Vestal New York 13850, (US)
Gregor, Steven Lee, 628 Church Street, Endicott New York 13760, (US)
Reeve, Stephen Michael, 113 E. Wendell Street, Endicott New York 13760, (US)
LEGAL REPRESENTATIVE:
Schafer, Wolfgang, Dipl.-Ing. (62021), IBM Deutschland Informationssysteme GmbH Patentwesen und Urheberrecht, D-70548 Stuttgart, (DE)
PATENT (CC, No, Kind, Date): EP 348628 A2 900103 (Basic)
EP 348628 A3 910102
APPLICATION (CC, No, Date): EP 89107502 890426;
PRIORITY (CC, No, Date): US 212561 880628
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS (V7): G06F-012/08;
CITED PATENTS (EP A): GB 2178205 A; GB 2178205 A; GB 2178205 A; GB 2056135 A; GB 2011667 A; EP 220990 A; US 4323968 A
CITED REFERENCES (EP A):
PROCEEDINGS OF THE 1987 INTERNATIONAL CONFERENCE ON PARALLEL PROCESSING, New York, 17th - 21st August 1987, pages 258-261; J.-L. BAER et al.: "Architectural choices for multilevel cache hierarchies";

ABSTRACT EP 348628 A2
Multi level cache **storage** system for a multiprocessor system in which each processor has a level one cache **storage** unit which interfaces with a level two cache unit and main **storage** unit shared by all processors. The multiprocessors share the level two cache according to a priority algorithm. When data in the level two cache is updated, corresponding data in level one caches is invalidated until it is updated.
ABSTRACT WORD COUNT: 73

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	900103	A2	Published application (A1with Search Report ;A2without Search Report)
Examination:	900613	A2	Date of filing of request for examination: 900419
Search Report:	910102	A3	Separate publication of the European or International search report
Change:	930331	A2	Representative (change)
Change:	930512	A2	Representative (change)
Change:	940914	A2	Representative (change)
Examination:	941130	A2	Date of despatch of first examination report: 941013
Withdrawal:	961227	A2	Date on which the European patent application was deemed to be withdrawn: 960702

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	435
SPEC A	(English)	EPABF1	73040

Total word count - document A 73475
Total word count - document B 0
Total word count - documents A + B 73475

Cache storage **system.**

...ABSTRACT A2
Multi level cache **storage** system for a multiprocessor system in which each processor has a level one cache **storage** unit which interfaces with a level two cache unit and main **storage** unit shared by all processors. The multiprocessors share the level two cache according to a...

...SPECIFICATION of processors, each of which may at some point in time require access to main **memory** . This requirement may arise simultaneously with respect to **two** or more of the processors in the multiprocessing system. Such systems also often comprise intermediate level **caches** for temporarily storing instructions and data. Simultaneous access to the intermediate level **caches** may also be required by **two** or more of the processors of the multiprocessing system. When such simultaneous access requirements arise...

...is also required. All of these requirements arise as a result of use of a **plurality** of **processors** and a single main **memory** in conjunction with intermediate level **caches** . As a result, an apparatus is needed to police and otherwise maintain accurate control over access to main **memory** and the caches. In this application, this appratus is termed a "Bus Switching Unit" (BSU...

...operations. This line buffer, when full, will cause a block transfer of data to L3 **memory** to occur. Therefore, **memory** operations are reduced from a number of individual store operations to a much smaller **number** of line transfers.
The instruction **cache** /data **cache** 18 are each 16K byte **caches** . The interface to the **storage** controller 12 is 8 bytes wide; thus, an inpage operation from the **storage** controller 12 takes 8 data transfer cycles. The data cache 18 is a "store through...

...storage controller 12 via an 8-byte bus. The subsystem 14 comprises three 64-byte **buffers** used to synchronize data coming from the integrated I/O subsystem 14 with the **storage** controller 12. That is, the instruction/execution unit 20 and the I/O subsystem 14 operate on **different** clocks, the synchronization of the two clocks being achieved by the three 64-byte **buffer** structure.
The multisystem channel communication unit 24 is a 4-port channel to channel adapter...

...integrated I/O subsystem 14, to shared channel processor A (SHCP-A) 28a, to shared **channel** processor B (SHCP-B) 28b, and to **three** **processors** : a first processor including instruction/data **caches** 18a and instruction/execution units/control store 20a, a second processor including instruction/data **caches** 18b and instruction/execution units/control store 20b, and a third processor including instruction/data ...

...18c are termed "L1" caches. The cache in the BSU 26 is termed the L2 **cache** 26a, and the main **memory** 10a/10b is termed the L3 **memory** .
The BSU 26 connects the **three** **processors** 18a/20a, 18b/20b, and 18c/20c, two L3 **memory** ports 10a/10b, two shared channel processors 28, and an integrated I/O subsystem 14...

...requests to be handled, such as requests from each of the three processors to L3 **memory** , or requests from the I/O subsystem 14 or shared channel processors, circuits which operate...

...figure 1 is identical to the memory cards 10a/10b of figure 2. The two

memory cards 10a/10b of figure 2 are accesses in parallel.
The shared channel processor 28 is connected to the BSU 26 via two ports , each port being an 8-byte interface. The shared channel processor 28 is operated at...cache storage 18b; a second vector processing unit 22b connected to the second L1 cache storage 18b; a third processing unit 20c, including an instruction unit, an execution unit, a control store, connected to the third L1 cache storage 18c; and a third vector processing unit 22c connected to the third L1 cache storage 18c. A shared channel processor A 28a and a shared channel processor B 28b are jointly connected to the storage subsystem 10, and an integrated adapter subsystem 14,16 is also connected to the storage subsystem 10.
Referring to figure 5, the storage subsysten 10 of figures 2 and 4 is illustrated.
In figure 5, the storage subsystem...

...L4 port 1 10d cornected to the L2 cache/bus switching unit 26a/26, a memory control 10e connected to the L2 control 10k, a bus switching unit control 10f connected to the L2 cache /bus switching unit 26a/26 and to the memory control 10e, storage channel data buffers 10g connected to the bus switching unit control 10f and to the L2 cache /bus switching unit 26a/26, an address/key control 10h connected to the memory control 10e and to the L2 control 10k, L3 storage keys 10i connected to the address/key control 10h, and a channel L2 cache directory...L3. The ports are divided into even and odd 128-byte L3 lines. The L3 storage interface is a 16-byte bi-directional, multiplexed command/address and data buss. The memory controller can have two parallel operations active, one to each port. From the processor viewpoint, all accesses to L3 storage are for inpage and outpage requests using full 128-byte line operations. From the channel viewpoint, either partial (one to 128 bytes) or full line operations are available to L3 storage . Storage reconfiguration is supported in anticipation of the two-frame system. The support consists of arrays , called subincrement frame maps and memory maps, which allow another level of address translation. This address translation is from absolute to...source of the 128 bytes of data to be moved into the specified L4 extended storage line and releases it upon completion of this operation. For PGOUT, transfer L3 line to memory buffer is the first storage command. The implementation outlined does not guarantee that another processor or channels cannot access the L3 line to be moved in the interval between when the processor issues the first storage command and memory control activates this storage command to transfer the allocated memory buffer contents to L4 for the PGOUT instruction. This...source of the 128 bytes of data to be moved into the specified L3 processor storage line and releases it upon completion of this operation. For PGIN, transfer L4 line to memory buffer is the first storage command. The implementation outlined does not guarantee that another processor or channels cannot access the L3 line to be loaded in the interval between when the processor issues the first storage command and memory control activates this storage command to transfer the allocated memory buffer contents to L3 for the PGIN instruction. This
...

? t21/5,k/29

21/5,K/29 (Item 29 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00295521
Identification of data storage devices.
Identifizierung von Datenspeicherungseinrichtungen.
Identification de dispositif de stockage de donnees.
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB)
INVENTOR:

Beardsley, Brent C., 9533 East Stella Drive, Tucson Arizona 85730, (US)
Boulia, Lawrence Herbert, 12149 McDonald Chapel Drive, Gaithersburg, Md. 20878, (US)
Vosacek, Robert Haver, 11205 Chuckwagon Circle, Tucson Arizona 85749, (US)
LEGAL REPRESENTATIVE:
Burt, Roger James, Dr. (52152), IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)
PATENT (CC, No, Kind, Date): EP 303855 A2 890222 (Basic)
EP 303855 A3 900207
EP 303855 B1 930616
APPLICATION (CC, No, Date): EP 88112032 880726;
PRIORITY (CC, No, Date): US 87331 870820
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS (V7): G06F-013/12; G06F-011/16; G06F-003/06; G06F-011/20;
CITED PATENTS (EP A): EP 59838 A; US 4207609 A; US 4162520 A; EP 62463 A; EP 81056 A; EP 205965 A; US 4648036 A

ABSTRACT EP 303855 A2
A technique is described for assuring the global identification and management of interchangeable data **storage** devices in a data processing system, assuring the integrity of data **storage** devices after shutdowns or failures and providing these capabilities without changing any current system or application software on the host. This technique also provides high availability of data **storage** devices by swapping a failing data **storage** device with a good data **storage** device without host intervention. To better understand the embodiment of the present invention hereinafter disclosed, it will be necessary to discuss some of the details of this prior art DASD system operation. When the Host CPU requires information, it requests it by requesting a specific channel, controller and DASD actuator. The channel is identified by a number which is a one byte hexadecimal number, the controller by a four bit hexadecimal number and the DASD actuator number by a four bit hexadecimal number. For example, if the host CPU were to send a two byte hexadecimal address 0111 in a start input/output operation (I/O), then actuator one, attached to controller one, attached to channel one would prepare for I/O and send the host a ready signal. Since the mapping down and back is the same, the original transaction header can be used to determine the path back to the host. Any host program accessing the DASD could send the header described above to uniquely define the DASD actuator to access.
ABSTRACT WORD COUNT: 243

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	890222	A2	Published application (A1with Search Report ;A2without Search Report)
Examination:	890816	A2	Date of filing of request for examination: 890619
Search Report:	900207	A3	Separate publication of the European or International search report
Examination:	920722	A2	Date of despatch of first examination report: 920609
Change:	920930	A2	Representative (change)
Grant:	930616	B1	Granted patent
Change:	930922	B1	Representative (change)
Oppn None:	940608	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	763
CLAIMS B	(German)	EPBBF1	635
CLAIMS B	(French)	EPBBF1	886
SPEC B	(English)	EPBBF1	3933
Total word count - document A			0
Total word count - document B			6217

Total word count - documents A + B 6217

Identification of data storage devices.

...ABSTRACT A2

A technique is described for assuring the global identification and management of interchangeable data **storage** devices in a data processing system, assuring the integrity of data **storage** devices after shutdowns or failures and providing these capabilities without changing any current system or application software on the host. This technique also provides high availability of data **storage** devices by swapping a failing data **storage** device with a good data **storage** device without host intervention. To better understand the embodiment of the present invention hereinafter disclosed...

...SPECIFICATION function to access groups is particularly useful in interleaved channel transfers for ensuring subsystem integrity.

Accordingly , the present invention provides a method for managing a data **processing** system having a host system, an attached controller comprising a set **of** **storage** **paths** attached to a **cache** , **a** data **storage** device controller, and a nonvolatile **storage** , and a **memory** containing an **array** structure comprising a status table containing the status records of the data **storage** devices, the system generating a global status record combining the status records of the controller...IBM 3880 Model 23 DASD Controller. The IBM 3880 Model 23 contains a high speed **cache** and two **storage** directors 41 and **49** , each **with** a single **storage** **path** for **independent** **control** of attached DASD devices 53. The IBM 3880 controller is described in IBM publication, IBM 3880 **Storage** Control Model 23 Description, GC32-0082. A good example of a DASD device 0-3...

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File 347:JAPIO Dec 1976-2006/Jan(Updated 061009)
         (c) 2006 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2006/ 200643
         (c) 2006 European Patent Office
File 349:PCT FULLTEXT 1979-2006/UB=20061026UT=20061019
         (c) 2006 WIPO/Thomson
File 350:Derwent WPIX 1963-2006/UD=200669
         (c) 2006 The Thomson Corporation

Set     Items   Description
S1       8034   AU='INOUE Y':AU='INOUE Y W O'
S2        713   AU='INOUE YASUO':AU='INOUE YASUO 4 3 37 KATAHIRA ASAO KU K-
            AWASAKI S'
S3       8461   S1:S2
S4      98585   DISK()DRIVE? ?
S5       1062   S4(10N)CACHE?
S6        350   S5(10N)CONTROL????
S7         10   S3 AND S6
? t7/69/all
>>>Format 69 is not valid in file 348

 7/69/1     (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0013974615  - Drawing available
WPI ACC NO: 2004-155470/
Related WPI Acc No: 1995-366079; 1998-008340; 1999-526949; 2002-215337;
  2004-155465; 2004-155466; 2004-155467; 2004-155468; 2004-155469
XRPX Acc No: N2004-124385
Storage system such as magnetic disk sub-system for computer, has cache
units coupled to channel units of host and control units of magnetic disk
drive
Patent Assignee: HITACHI LTD  (HITA)
Inventor:  INOUE Y
Patent Family (1 patents,  1 countries)
Patent                          Application
Number          Kind   Date     Number          Kind   Date     Update
US 20040010659   A1  20040115  US 1992984763    A  19921203  200415  B
                                 US 1995502045    A  19950713
                                 US 1997902362    A  19970729
                                 US 1999379635    A  19990824
                                 US 2001819636    A  20010329
                                 US 2003614864    A  20030709

Priority Applications (no., kind, date): JP 1991322965  A  19911206

Patent Details
Number         Kind  Lan   Pg  Dwg  Filing Notes
US 20040010659   A1  EN    11    7  Continuation of application  US
   1992984763
                                    Continuation of application  US
   1995502045
                                    Division of application  US 1997902362

                                    Continuation of application  US
   1999379635
                                    Continuation of application  US
   2001819636
                                    Continuation of patent  US 5459856
                                    Continuation of patent  US 5689729
                                    Division of patent  US 5951655

  Alerting Abstract US A1
  NOVELTY - The system has cache units (80,81) independently connected to
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multiple channel units (60,61) and control units (70,71). The channel units control data transfer to and from the central processing unit (1). The multiple control units control data transfer to and from the magnetic disk drive.

USE - Storage system such as magnetic disk sub-system used for general purpose computer system.

ADVANTAGE - Since the access paths to cache units are multiplexed. The reliability of cache function and its tolerance to failures are improved.

DESCRIPTION OF DRAWINGS - The figure shows the block diagram of the external storage sub system.

1 CPU
60,61 channel unit
70,71 control unit
80,81 cache unit
80a,80b access lines

Title Terms/Index Terms/Additional Words: STORAGE; SYSTEM; MAGNETIC; DISC; SUB; COMPUTER; CACHE; UNIT; COUPLE; CHANNEL; HOST; CONTROL; DRIVE

Class Codes
International Classification (Main): G06F-012/00

File Segment: EPI;
DWPI Class: T01; T03
Manual Codes (EPI/S-X): T01-C01A; T01-H03A; T01-H07A; T03-A08A1C; T03-A10E; T03-N01

7/69/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0013974614 - Drawing available
WPI ACC NO: 2004-155469/
Related WPI Acc No: 1995-366079; 1998-008340; 1999-526949; 2002-215337; 2004-155465; 2004-155466; 2004-155467; 2004-155468; 2004-155470
XRPX Acc No: N2004-124384

Storage system in computer, links control units with respective cache units through separate paths so as to equalize number of paths with respect to number of control units

Patent Assignee: HITACHI LTD (HITA)
Inventor: INOUE Y

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 20040010658	A1	20040115	US 1992984763	A	19921203	200415 B
			US 1995502045	A	19950713	
			US 1997902362	A	19970729	
			US 1999379635	A	19990824	
			US 2001819636	A	20010329	
			US 2003614859	A	20030709	

Priority Applications (no., kind, date): JP 1991322965 A 19911206

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20040010658	A1	EN	11	7	Continuation of application US 1992984763
					Continuation of application US 1995502045
					Division of application US 1997902362
					Continuation of application US 1999379635
					Continuation of application US

2001819636

Continuation of patent US 5459856
Continuation of patent US 5689729
Division of patent US 5951655

Alerting Abstract US A1

NOVELTY - The control units (70,71) exchange data between cache units (80,81) that stores data sent from the channel units (60,61). The control units are linked with respective cache units through individual paths so that the number of paths is equal to the total number of control units.

USE - E.g. magnetic disk system for use in general purpose computer.

ADVANTAGE - The cache function and performance in the disk control unit are improved by coupling the cache units and channel units or control units easily and smoothly.

DESCRIPTION OF DRAWINGS - The figure shows a block diagram of the external storage subsystem.

1 CPU
2 disk controller
3 magnetic disk drive
60,61 channel units
70,71 control units
80,81 cache units

Title Terms/Index Terms/Additional Words: STORAGE; SYSTEM; COMPUTER; LINK; CONTROL; UNIT; RESPECTIVE; CACHE; THROUGH; SEPARATE; PATH; SO; NUMBER; RESPECT

Class Codes
International Classification (Main): G06F-012/00

File Segment: EPI;
DWPI Class: T01; T03
Manual Codes (EPI/S-X): T01-C01A; T01-H03A; T01-H07A; T03-A08A1C; T03-A10E; T03-N01

7/69/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0013974613 - Drawing available
WPI ACC NO: 2004-155468/200415
Related WPI Acc No: 1995-366079; 1998-008340; 1999-526949; 2002-215337; 2004-155465; 2004-155466; 2004-155467; 2004-155469; 2004-155470
XRPX Acc No: N2004-124383

External storage sub-system such as magnetic disk sub-system has cache units connected to control units and channel units through respective paths

Patent Assignee: HITACHI LTD (HITA)
Inventor: **INOUE Y**

Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
US 20040010642	A1	20040115	US 1992984763	A	19921203	200415	B
			US 1995502045	A	19950713		
			US 1997902362	A	19970729		
			US 1999379635	A	19990824		
			US 2001819636	A	20010329		
			US 2003614863	A	20030709		
US 6981067	B2	20051227	US 1992984763	A	19921203	200603	E
			US 1995502045	A	19950713		
			US 1997902362	A	19970729		
			US 1999379635	A	19990824		
			US 2001819636	A	20010329		
			US 2003614863	A	20030709		

Priority Applications (no., kind, date): JP 1991322965 A 19911206

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20040010642	A1	EN	11	7	Continuation of application US 1992984763 Continuation of application US 1995502045 Division of application US 1997902362 Continuation of application US 1999379635 Continuation of application US 2001819636 Continuation of patent US 5459856 Continuation of patent US 5689729 Division of patent US 5951655
US 6981067	B2	EN			Continuation of application US 1992984763 Continuation of application US 1995502045 Division of application US 1997902362 Continuation of application US 1999379635 Continuation of application US 2001819636 Continuation of patent US 5459856 Continuation of patent US 5689729 Division of patent US 5951655 Continuation of patent US 6745261

Alerting Abstract US A1

NOVELTY - The cache units (80,81) that store the data from the channel units (60,61) are connected to the control units (70,71) and the channel units through the respective paths.

USE - External storage sub-system such as magnetic disk sub-system used with general purpose computer system.

ADVANTAGE - Since the cache units and the access paths to the cache units are multiplexed, probability of maintaining the cache function is enhanced and reliability of the external storage sub-system and the tolerance to the failures are improved.

DESCRIPTION OF DRAWINGS - The figure shows the block diagram of the external storage sub-system.

1 central processing unit
2 disk controller
3 magnetic disk drive
4 channel interface
5 control interface
60,61 channel units
70,71 control units
80,81 cache units
111 control processor

Title Terms/Index Terms/Additional Words: EXTERNAL; STORAGE; SUB; SYSTEM; MAGNETIC; DISC; CACHE; UNIT; CONNECT; CONTROL; CHANNEL; THROUGH; RESPECTIVE; PATH

Class Codes

International Classification (Main): G06F-013/00, G06F-003/00

File Segment: EPI;
DWPI Class: T01; T03
Manual Codes (EPI/S-X): T01-C01A; T01-H03A; T03-A08A1C; T03-A10A; T03-N01

7/69/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0013974612 - Drawing available
WPI ACC NO: 2004-155467/200415
Related WPI Acc No: 1995-366079; 1998-008340; 1999-526949; 2002-215337; 2004-155465; 2004-155466; 2004-155468; 2004-155469; 2004-155470
XRPX Acc No: N2004-124382

Magnetic disk subsystem in computer system, has cache units connected to channel units and control units, that respectively control data transfer to/from central processor and magnetic disk drive

Patent Assignee: HITACHI LTD (HITA)
Inventor: INOUE Y

Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 20040010641	A1	20040115	US 1992984763	A	19921203	200415 B
			US 1995502045	A	19950713	
			US 1997902362	A	19970729	
			US 1999379635	A	19990824	
			US 2001819636	A	20010329	
			US 2003614862	A	20030709	
US 7010623	B2	20060307	US 1992984763	A	19921203	200618 E
			US 1995502045	A	19950713	
			US 1997902362	A	19970729	
			US 1999379635	A	19990824	
			US 2001819636	A	20010329	
			US 2003614862	A	20030709	

Priority Applications (no., kind, date): JP 1991322965 A 19911206

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20040010641	A1	EN	12	7	Continuation of application US 1992984763
					Continuation of application US 1995502045
					Division of application US 1997902362
					Continuation of application US 1999379635
					Continuation of application US 2001819636
					Continuation of patent US 5459856
					Continuation of patent US 5689729
					Division of patent US 5951655
US 7010623	B2	EN			Continuation of application US 1992984763
					Continuation of application US 1995502045
					Division of application US 1997902362
					Continuation of application US 1999379635
					Continuation of application US 2001819636
					Continuation of patent US 5459856
					Continuation of patent US 5689729
					Division of patent US 5951655
					Continuation of patent US 6745261

Alerting Abstract US A1
NOVELTY - The cache units (80,81) and non-volatile memory units (90,91)

are provided in a disk controller 92) located between a central processor (1) and a magnetic disk drive (3). The channel units (60,61) controlling the data transfer to/from the processor, and the **control** units **controlling** the data transfer to/from the **disk drive** are independently connected to the **cache** units through access lines (81a,81b-81d,90a-90d).

USE - Storage system e.g. magnetic disk subsystem in general purpose computer system.

ADVANTAGE - The cache function and performance of the disk control unit are improved by coupling the cache units to the channel units and the control units. The tolerance to the failures and reliability of cache function are increased by multiplexing the cache units and the access paths to the cache units.

DESCRIPTION OF DRAWINGS - The figure shows the block diagram of an external storage subsystem.

1 central processing unit
2 disk controller
3 disk drive
60,61 channel units
70,71 control units
80,81 cache units
90,91 memory units
81a,81b-81d,90a-90d access lines

Title Terms/Index Terms/Additional Words: MAGNETIC; DISC; SUBSYSTEM; COMPUTER; SYSTEM; CACHE; UNIT; CONNECT; CHANNEL; CONTROL; RESPECTIVE; DATA; TRANSFER; CENTRAL; PROCESSOR; DRIVE

Class Codes
International Classification (Main): G06F-013/00
International Classification (+ Attributes)
IPC + Level Value Position Status Version
G06F-0003/00 A I F B 20060101

File Segment: EPI;
DWPI Class: T01; T03
Manual Codes (EPI/S-X): T01-C01A; T01-H03A; T01-H05B2; T01-H07A; T03-A08A1C ; T03-A10E1; T03-N01

7/69/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0013974611 - Drawing available
WPI ACC NO: 2004-155466/200415
Related WPI Acc No: 1995-366079; 1998-008340; 1999-526949; 2002-215337; 2004-155465; 2004-155467; 2004-155468; 2004-155469; 2004-155470
XRPX Acc No: N2004-124381

Magnetic disk subsystem for computer, has channel units and control units which are independently connected to cache units and non-volatile memory units through data buses and access lines

Patent Assignee: HITACHI LTD (HITA)
Inventor: INOUE Y
Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 20040010640	A1	20040115	US 1992984763	A	19921203	200415 B
			US 1995502045	A	19950713	
			US 1997902362	A	19970729	
			US 1999379635	A	19990824	
			US 2001819636	A	20010329	
			US 2003614861	A	20030709	
US 6981066	B2	20051227	US 1992984763	A	19921203	200603 E
			US 1995502045	A	19950713	
			US 1997902362	A	19970729	
			US 1999379635	A	19990824	

US 2001819636 A 20010329
US 2003614861 A 20030709

Priority Applications (no., kind, date): JP 1991322965 A 19911206

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20040010640	A1	EN	12	7	Continuation of application US 1992984763 Continuation of application US 1995502045 Division of application US 1997902362 Continuation of application US 1999379635 Continuation of application US 2001819636 Continuation of patent US 5459856 Continuation of patent US 5689729 Division of patent US 5951655
US 6981066	B2	EN			Continuation of application US 1992984763 Continuation of application US 1995502045 Division of application US 1997902362 Continuation of application US 1999379635 Continuation of application US 2001819636 Continuation of patent US 5459856 Continuation of patent US 5689729 Division of patent US 5951655 Continuation of patent US 6745261

Alerting Abstract US A1

NOVELTY - The channel units (60,61) for controlling data transfer to and from a central processing unit (CPU) (1), and control units (70,71) for **controlling** data transfer to and from magnetic **disk drive** (3), are independently connected to **cache** units (80,81) and non-volatile memory units (90,91) through data buses and access lines.

DESCRIPTION - An INDEPENDENT CLAIM is also included for storage unit.

USE - Magnetic disk subsystem for computer.

ADVANTAGE - The subsystem which has high tolerance to failure and highly reliable cache function is realized.

DESCRIPTION OF DRAWINGS - The figure shows a block diagram of the external storage device.

1 CPU
3 magnetic disk drive
60,61 channel units
70,71 control units
80,81 cache units
90,91 non-volatile memory units
60A,60B,61A,61B,70A,70B,71A,71B data buses
80a-80d,81a-81d,90a-90d,91a-91d access lines

Title Terms/Index Terms/Additional Words: MAGNETIC; DISC; SUBSYSTEM; COMPUTER; CHANNEL; UNIT; CONTROL; INDEPENDENT; CONNECT; CACHE; NON; VOLATILE; MEMORY; THROUGH; DATA; BUS; ACCESS; LINE

Class Codes

International Classification (Main): G06F-013/00, G06F-003/00

File Segment: EPI;
DWPI Class: T01; T03

Manual Codes (EPI/S-X): T01-C01A; T01-H03A; T03-A08A1C; T03-N01

7/69/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0013974610 - Drawing available
WPI ACC NO: 2004-155465/200415
Related WPI Acc No: 1995-366079; 1998-008340; 1999-526949; 2002-215337; 2004-155466; 2004-155467; 2004-155468; 2004-155469; 2004-155470
XRPX Acc No: N2004-124380
External storage subsystem e.g. magnetic disk subsystem includes number of data buses equal to number of channel units for connecting channel units to respective cache units
Patent Assignee: HITACHI LTD (HITA)
Inventor: INOUE Y
Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 20040010639	A1	20040115	US 1992984763	A	19921203	200415 B
			US 1995502045	A	19950713	
			US 1997902362	A	19970729	
			US 1999379635	A	19990824	
			US 2001819636	A	20010329	
			US 2003614860	A	20030709	
US 7099960	B2	20060829	US 1987902362	A	19870729	200657 E
			US 1992984763	A	19921203	
			US 1995502045	A	19950713	
			US 1999379635	A	19990824	
			US 2001819636	A	20010329	
			US 2003614860	A	20030709	

Priority Applications (no., kind, date): JP 1991322965 A 19911206

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20040010639	A1	EN	11	7	Continuation of application US 1992984763
					Continuation of application US 1995502045
					Division of application US 1997902362
					Continuation of application US 1999379635
					Continuation of application US 2001819636
					Continuation of patent US 5459856
					Continuation of patent US 5689729
					Division of patent US 5951655
US 7099960	B2	EN			Division of application US 1987902362
					Continuation of application US 1992984763
					Continuation of application US 1995502045
					Continuation of application US 1999379635
					Continuation of application US 2001819636
					Continuation of patent US 5459856
					Continuation of patent US 5689729
					Division of patent US 5951655
					Continuation of patent US 6745261

Alerting Abstract US A1

NOVELTY - Multiple channel units (60,61) receive data from an upper level system for transfer to cache units (800,801). The control units (70,71) transfer or receive data to and from the cache units for storing in a magnetic disk drive (3). The channel units are connected to the respective cache units through respective data buses (60g,61g,60j,61j). The number of data buses is equal to the number of the channel units.

USE - External storage subsystem e.g. magnetic disk subsystem used with general purpose computer system.

ADVANTAGE - The cache function and performance in the disk control unit are improved by coupling independently and directly the channel units of the host to the cache units through respective data buses in a simple manner. The cache units and the access paths are multiplexed to achieve high tolerance to failures and a highly reliable cache function.

DESCRIPTION OF DRAWINGS - The figure shows a block diagram of the external storage subsystem.

3 magnetic disk drive
60,61 channel units
60g,60j,61g,61j data buses
70,71 control units
800,801 cache units
900,901 non-volatile memory units

Title Terms/Index Terms/Additional Words: EXTERNAL; STORAGE; SUBSYSTEM; MAGNETIC; DISC; NUMBER; DATA; BUS; EQUAL; CHANNEL; UNIT; CONNECT; RESPECTIVE; CACHE

Class Codes
International Classification (+ Attributes)

IPC + Level Value	Position	Status	Version
G06F-0012/08 A I	R		20060101
G11C-0029/00 A I	R		20060101
G06F-0003/00 A I F	B		20060101
G06F-0012/08 C I	R		20060101
G11C-0029/00 C I	R		20060101

File Segment: EPI;
DWPI Class: T01; T03
Manual Codes (EPI/S-X): T01-C01A; T01-C07C2; T01-H03A; T03-A08A1C; T03-N01

7/69/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0012274675 - Drawing available
WPI ACC NO: 2002-215337/
Related WPI Acc No: 1995-366079; 1998-008340; 1999-526949; 2004-155465; 2004-155466; 2004-155467; 2004-155468; 2004-155469; 2004-155470
XRPX Acc No: N2002-164898

External storage subs-system such as magnetic disk sub-system in computer system, has access paths to permit access to cache memories to control data transfer between CPU and magnetic disk drive

Patent Assignee: HITACHI LTD (HITA); INOUE Y (INOU-I)
Inventor: INOUE Y
Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
US 20010014923	A1	20010816	US 1992984763	A	19921203	200227	B
			US 1995502045	A	19950713		
			US 1997902362	A	19970729		
			US 1999379635	A	19990824		
			US 2001819636	A	20010329		
US 6745261	B2	20040601	US 2001819636	A	20010329	200436	E

Priority Applications (no., kind, date): US 2001819636 A 20010329; JP 1991322965 A 19911206

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20010014923	A1	EN	11	7	Continuation of application US 1992984763
					Continuation of application US 1995502045
					Division of application US 1997902362
					Continuation of application US 1999379635
					Continuation of patent US 5459856
					Continuation of patent US 5689729
					Division of patent US 5951655

Alerting Abstract US A1

NOVELTY - A memory controller including cache memories, stores data from the central processing unit (1) or from magnetic disk drive (3) temporarily in non-volatile or volatile semiconductor memory. Multiple fault tolerant access paths permit access to **cache** memories from CPU for magnetic **disk drive** to **control** data transfer between the CPU and disk drive.

USE - E.g. magnetic disk sub-system in computer system.

ADVANTAGE - Has high tolerance to failures and high reliable cache function by multiplexing both cache units and access paths to the cache units.

DESCRIPTION OF DRAWINGS - The figure shows the block diagram of external storage sub-system.

1 Central processing unit

3 Magnetic disk drive

Title Terms/Index Terms/Additional Words: EXTERNAL; STORAGE; SYSTEM; MAGNETIC; DISC; SUB; COMPUTER; ACCESS; PATH; PERMIT; CACHE; MEMORY; CONTROL; DATA; TRANSFER; CPU; DRIVE

Class Codes

International Classification (Main): G06F-013/14, G06F-003/00

File Segment: EPI;
DWPI Class: T01; T03
Manual Codes (EPI/S-X): T01-C01A; T01-H01B1; T01-H03A; T01-H05B; T03-A08A1C ; T03-A10E1; T03-N01

7/69/8 (Item 8 from file: 350)

0009579412 - Drawing available
WPI ACC NO: 1999-526949/
Related WPI Acc No: 1995-366079; 1998-008340; 2002-215337; 2004-155465; 2004-155466; 2004-155467; 2004-155468; 2004-155469; 2004-155470
XRPX Acc No: N1999-390316

External storage subsystem in general purpose computer system

Patent Assignee: HITACHI LTD (HITA)
Inventor: INOUE Y

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 5951655	A	19990914	US 1992984763	A	19921203	199944 B
			US 1995502045	A	19950713	
			US 1997902362	A	19970729	

Priority Applications (no., kind, date): JP 1991322965 A 19911206

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5951655	A	EN	12	7	Continuation of application US 1992984763
					Continuation of application US 1995502045
					Continuation of patent US 5459856
					Continuation of patent US 5689729

Alerting Abstract US A

NOVELTY - Several channel units (60,61) and control units (70,71) of memory controller perform independent access of the host and the rotating storage device to cache memories, as set of access lines (80a-80d, 81a-81d, 90a-90d, 91a-91d) independently connects the channel units and control units to cache memories.

DESCRIPTION - Several cache memories in memory controller, temporarily store the data transferred between rotating storage device of the system and the host. The channel units (60,61) controls data transfer at the host while the control units (70,71) controls data transfer at the rotating storage device. Several cache memories of the memory controller includes volatile and nonvolatile semiconductor memories. The function of both channel and control units are controlled by respective control processors.

USE - For magnetic disk subsystem in general purpose computer systems etc.

ADVANTAGE - The system has high tolerance to failures and has highly reliable cache function by provision of the databus structure between cache memories and channel and control units.

DESCRIPTION OF DRAWINGS - The figure shows the block diagram of the external storage subsystem.

60,61 Channel units
70,71 Control units
80a-80d, 81a-81d, 90a-90d, 91a-91d Access lines

Title Terms/Index Terms/Additional Words: EXTERNAL; STORAGE; SUBSYSTEM; GENERAL; PURPOSE; COMPUTER; SYSTEM

Class Codes

International Classification (Main): G06F-013/40

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-H07A

7/69/9 (Item 9 from file: 350)

0008479405 - Drawing available
WPI ACC NO: 1998-008340/
Related WPI Acc No: 1995-366079; 1999-526949; 2002-215337; 2004-155465; 2004-155466; 2004-155467; 2004-155468; 2004-155469; 2004-155470
XRPX Acc No: N1998-006637

Magnetic disk cache subsystem - has several independent access paths and external memory control with several channels to control transfer of data to and from disk and several access paths to cache

Patent Assignee: HITACHI LTD (HITA)
Inventor: INOUE Y

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 5689729	A	19971118	US 1992984763	A	19921203	199801 B
			US 1995502045	A	19950713	

Priority Applications (no., kind, date): JP 1991322965 A 19911206

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5689729	A	EN	12	7	Continuation of application US 1992984763
					Continuation of patent US 5459856

Alerting Abstract US A

The storage subsystem includes a disk for storing data from a host and sending data to the host in response to a request from the host. A memory controller includes several cache memories for temporarily storing the data transferred between the host and the disk. A number of channel units control data transfer to and from the host. Several control units for control data transfer to and from the disk. Several access paths permit independent access to the cache memories from the host and from the disk. The access paths include a number of common data buses. Each data bus is coupled to each channel unit, each cache memory and each control unit, for controlling data transfer between the host and the disk.

A first channel unit has a first access line connected to a first data bus and a second access line connected to a second data bus. A first control units has a first access line connected to the first data bus and a second access line connected to the second data bus. A second channel unit has a first access line connected to the first data bus and a second access line connected to the second data bus. A second control unit has a first access line connected to the first data bus and a second access line connected to the second data bus. Each of the cache memories has a first access line connected to the first data bus and a second access line connected to the second data bus.

ADVANTAGE - Allows connection of several cache units of host to several control units of disk. Increases tolerance to failure.

Title Terms/Index Terms/Additional Words: MAGNETIC; DISC; CACHE; SUBSYSTEM; INDEPENDENT; ACCESS; PATH; EXTERNAL; MEMORY; CONTROL; CHANNEL; TRANSFER; DATA

Class Codes

International Classification (Main): G06F-015/02

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-C01A; T01-H03A

7/69/10 (Item 10 from file: 350)

0007304872 - Drawing available
WPI ACC NO: 1995-366079/199547
Related WPI Acc No: 1998-008340; 1999-526949; 2002-215337; 2004-155465; 2004-155466; 2004-155467; 2004-155468; 2004-155469; 2004-155470
XRPX Acc No: N1995-270912

External storage subsystem for host independent cache access - has independent cache and non-volatile memory units with channel units controlling CPU and disk drive data transfer

Patent Assignee: HITACHI LTD (HITA)
Inventor: INOUE Y

Patent Family (9 patents, 2 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
US 5459856	A	19951017	US 1992984763	A	19921203	199547	B
JP 11338776	A	19991210	JP 1991322965	A	19911206	200009	E
			JP 1998346355	A	19911206		
JP 3451099	B2	20030929	JP 1991322965	A	19911206	200364	E

JP 2004005701	A	20040108	JP 1991322965	A	19911206	200405	E
			JP 2003156486	A	20030602		
JP 2004030645	A	20040129	JP 1991322965	A	19911206	200410	E
			JP 2003156485	A	20030602		
JP 2004070939	A	20040304	JP 2003156486	A	19911206	200417	NCE
			JP 2003189152	A	20030701		
JP 3742071	B2	20060201	JP 1991322965	A	19911206	200613	E
			JP 2003156485	A	20030602		
JP 3742072	B2	20060201	JP 1991322965	A	19911206	200613	E
			JP 2003156486	A	20030602		
JP 3742075	B2	20060201	JP 2003156486	A	19911206	200613	NCE
			JP 2003189152	A	20030701		

Priority Applications (no., kind, date): JP 2003189152 A 20030701; JP 2003156486 A 20030602; JP 2003156485 A 20030602; JP 1998346355 A 19911206; JP 1991322965 A 19911206

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5459856	A	EN	13	7	
JP 11338776	A	JA	9		Division of application JP 1991322965
JP 3451099	B2	JA	11		Previously issued patent JP 05158797
JP 2004005701	A	JA	27		Division of application JP 1991322965
JP 2004030645	A	JA	27		Division of application JP 1991322965
JP 2004070939	A	JA	14		Division of application JP 2003156486
JP 3742071	B2	JA	22		Division of application JP 1991322965
					Previously issued patent JP 2004030645
JP 3742072	B2	JA	21		Division of application JP 1991322965
					Previously issued patent JP 2004005701
JP 3742075	B2	JA	14		Division of application JP 2003156486
					Previously issued patent JP 2004070939

Alerting Abstract US A

The subsystem has a rotating storage device storing data from and sending data to a host in response to a signal from the host. A memory controller has cache memories temporarily storing data transferred between the host and storage device. Numerous channel units control data transfer to and from the host. Control units control data transfer to and from the storage device. The control units have numerous access paths permitting independent access to the host and storage device.

A first and second of the channel units have their data buses connected to access lines of the volatile and non-volatile memories. A first and second of the control units have their data buses connected to different access lines of the volatile and non-volatile memories.

ADVANTAGE - Attains highly reliable cache function. Provides high tolerance to failures.

Title Terms/Index Terms/Additional Words: EXTERNAL; STORAGE; SUBSYSTEM; HOST; INDEPENDENT; CACHE; ACCESS; MEMORY; UNIT; CHANNEL; CONTROL; CPU; DISC; DRIVE; DATA; TRANSFER

Class Codes

International Classification (Main): G06F-011/20, G06F-012/08, G06F-003/06
(Additional/Secondary): G06F-013/12, G06F-013/38
International Classification (+ Attributes)

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IPC + Level Value Position Status Version
  G06F-0012/08  A  I  F  B  20060101
  G06F-0012/08  A  I  L  B  20060101
  G06F-0013/12  A  I  L  B  20060101
  G06F-0013/38  A  I  L  B  20060101
  G06F-0003/06  A  I  L  B  20060101
  G06F-0003/06  A  I  F  B  20060101

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-G03; T01-H01B1; T01-H03A
?
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